

CLAIMS

What is claimed is:

- 1 1. A method for improving an input match in a circuit comprising:
 - 2 operating a cascode having an input signal port with an input signal
 - 3 impedance and further having a stage gain controlled by a level setting gain
 - 4 control voltage;
 - 5 and
 - 6 operating an impedance compensating circuit for changing a compensating
 - 7 impedance presented at the input signal port,
 - 8 wherein the impedance compensating circuit is controlled by
 - 9 the level setting gain control voltage and wherein the impedance
 - 10 compensating circuit is operable to counteract changes in the input
 - 11 signal impedance correlated with changes in the stage gain.
- 1 2. The method of claim 1 wherein:
 - 2 the impedance compensating circuit is connected in parallel with the
 - 3 input signal port.
- 1 3. The method of claim 1 wherein:
 - 2 the impedance compensating circuit is connected in series with the
 - 3 input signal port.
- 1 4. The method of claim 1 wherein:
 - 2 the impedance compensating circuit is connected in series-parallel with
 - 3 the input signal port.
- 1 5. The method of claim 1 wherein:
 - 2 the cascode is implemented using Gallium Arsenide transistors.

1 6. The method of claim 1 wherein:

2 the cascode is implemented using metal-oxide semiconductor
3 transistors formed as an integrated circuit.

1 7. The method of claim 1 wherein:

2 the cascode is implemented using devices selected from a list
3 consisting of metal-oxide semiconductor transistors, silicon bipolar transistors
4 and germanium transistors.

1 8. A circuit for processing a signal comprising:

2 a cascode having

3 a first transistor connected in a configuration selected from a
4 group consisting of a common gate configuration and a common base
5 configuration

6 and

7 a second transistor connected in a configuration selected from a
8 group consisting of a common source configuration, a common drain
9 configuration, a common emitter configuration and a common
10 collector configuration;

11 a gain controller operable to adjust a gain of the cascode in response to
12 a control signal; and

13 an impedance controller operable to adjust an input impedance of the
14 cascode with a loading impedance in response to the control signal;

15 whereby the circuit operates with input impedance
16 compensation.

1 9. The circuit of claim 8 wherein

2 the circuit is an amplifier.

1 10. The circuit of claim 8 wherein

2 the circuit is an amplifier that operates at a narrow band of frequencies
3 in the microwave region.

1 11. The circuit of claim 8 wherein
2 the circuit is implemented as a single integrated circuit.

1 12. The circuit of claim 8 wherein
2 the circuit is implemented using metal-oxide semiconductor
3 technologies.

1 13. The circuit of claim 8 wherein
2 the circuit is implemented using Gallium Arsenide technologies.

1 14. The circuit of claim 8 wherein
2 the impedance controller comprises an inverter.

1 15. The circuit of claim 8 wherein
2 the gain controller outputs a DC bias voltage that is applied to a control
3 terminal of the first transistor.

1 16. A circuit for processing a signal comprising:
2 a cascode having

3 a first transistor connected in a configuration selected from a
4 group consisting of a common gate configuration and a common base
5 configuration

6 and

7 a second transistor connected in a configuration selected from a
8 group consisting of a common source configuration, a common drain
9 configuration, a common emitter configuration and a common
10 collector configuration;

11 a controller operable to adjust a gain of the cascode in response to a
12 control signal and further operable to adjust an input impedance of the cascode
13 with a loading impedance in response to the control signal;
14 whereby the circuit operates with input impedance
15 compensation.

1 17. The circuit of claim 16 wherein
2 the circuit is an amplifier that operates at a narrow band of frequencies
3 in the microwave region.

1 18. The circuit of claim 16 wherein
2 the circuit is implemented as a single integrated circuit.

1 19. The circuit of claim 16 wherein
2 the circuit is implemented using metal-oxide semiconductor
3 technologies.

1 20. The circuit of claim 16 wherein
2 the circuit is implemented using Gallium Arsenide technologies.